A 20 MHz Low-Profile DC–DC Converter With Magnetic-Free Characteristics

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***Abstract*—This paper proposes a 20 MHz low-profile dc–dc converter with magnetic-free characteristics based on aircore planar inductors. The switch and diode of the proposed converter operate in soft-switching modes, which significantly reduces the switching loss. Furthermore, the parasitic capacitances are taken as part of corresponding resonant capacitors. A high-performance aircore inductor with a variable width and an optimal connecting angle is analyzed. The optimal parameters design method to achieve minimum winding resistance is derived in detail. The resonant driving method is adopted to reduce driving loss in a high-frequency condition. A 20 MHz prototype is built to verify the feasibility of the proposed converter.**

***Index Terms*—High frequency, low profile, magnetic-free.**

I. Introduction

WITH THE development of power electronic systems and power devices, advanced topologies, control methods, and high-frequency converters have begun attracting a lot of attention, aiming for a higher power density, lighter weight, and higher efficiency [1]–[8]. For instance, light-emitting diode (LED) has become one of the mainstream lighting sources because of their long lifetime and high efficacy. LED drivers are expected to be small in volume and have a low profile to achieve the desired flexibility and aesthetics as suitable to the fields, such as automotive lighting, indoor lighting, and aerospace lighting [9]–[15].

Many research works have been performed to identify the suitable converters and topologies of dc–dc systems. For nonisolated situations, boost converter, Cuk converter, and single ended primary inductor converter (SEPIC) converter are popular candidates. In [13], a Cuk converter with zero voltage switching (ZVS) soft-switching characteristics is proposed. However, extra switch and passive components are added. In [14], a modified SEPIC converter with enhanced voltage conversion ability is proposed. Its limitation is that it cannot operate in a soft-switching condition. The converters mentioned above usually operate at frequencies of around hundreds of kilohertz, and the system volumes and weights are mostly restricted by the magnetic components and electrolytic capacitors. As a result, they are not found suitable to be adopted in weight/volume sensitive situations.

To reduce the volume and weight of a power conversion system, the most effective approach is to promote the operating frequency. In high-frequency conditions, energy stored in the passive components during every period is very small. This results in a significant reduction in capacitance and inductance [16]–[27]. With a smaller inductance, the magnetic core can be avoided and aircore inductors can be used. For aircore inductors, the copper tracks on a printed circuit board (PCB) can be used as windings [28]–[33]. It can help to reduce the system profile, and make the system more compact and flexible. Furthermore, absence of a magnetic core significantly reduces the mass of inductors. In addition, the electrolytic capacitors can also be avoided to further reduce volume, weight and extend the lifespan. In high-frequency conditions, ceramic capacitors of NP0 or C0G with high performance can be adopted by leveraging the small energy transmission within each period.

There are limitations of frequency promotion, such as great switching loss, large winding loss, and parasitic component interference. In such high switching frequency conditions, the most challenging aspect is the high switching loss. Hence, the soft-switching operating mode of switch and diode is expected to reduce switching loss. In high-frequency conditions, the switch output capacitance and diode junction capacitance are at the comparable levels with the necessary resonant capacitors. Thus, these parasitic capacitances significantly impact system operating status and must be taken into consideration within design procedure [17]. An effective way to deal with these parasitic capacitances is to propose a suitable topology in which they can be a part of resonant capacitors. Taking advantage of the absorption, the value of discrete resonant capacitors can also be reduced. Besides semiconductor loss, the loss of inductor or transformer is also severe. Without core loss, the reduction of aircore magnetic component loss must start from optimizing the winding structure to achieve a smaller copper loss.

To solve the aforementioned problems, an advanced topology suitable for operating under high-frequency condition should be investigated. This paper proposes a 20 MHz dc–dc converter

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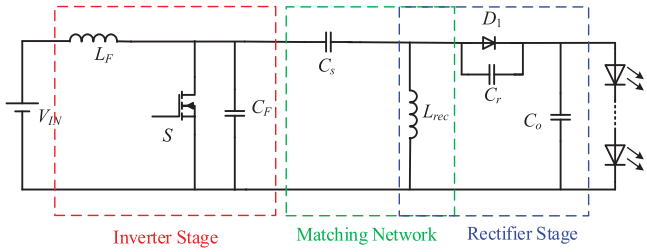


Fig. 1. Topology of the proposed dc–dc converter for LED driving system.

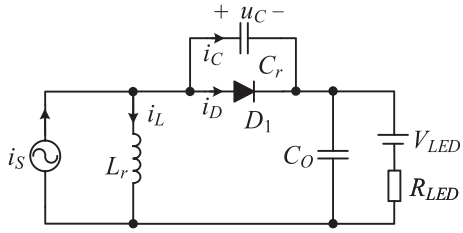


Fig. 2. Circuit of rectifier stage with LED as load.

along with the demonstration of the detailed design method of the proposed high-frequency system with soft switching modes of the switch and diode. This paper involves usage of aircore planar inductors with an optimal winding structure to reduce the winding loss. For the proposed dc–dc converter, the profile is greatly reduced, and the power density is greatly improved. The prototype adopts a pulsewidth modulation (PWM) type ON/OFF control method that modulates the effective operating time of the high-frequency signal. Its objective is to address the difficulty in adjusting the operating frequency or duty cycle in such a high frequency operating condition.

The paper is divided into five sections. Following the introduction in Section I, Section II includes the analysis of the circuit topology and system design method of the high frequency converter. Section III presents the optimal winding structure of aircore planar inductor by calculating the inductance and resistance in detail. In Section IV, the 20 MHz prototype with resonant driving method and ON/OFF control method is built and the experimental waveforms are given. Section V concludes this paper.

II. Analysis and Design of the Proposed Converter

A. Working Principle of the Converter

Fig. 1 shows the topology of the proposed converter. Here, LED is taken as an example of the load. When the load is resistor in other applications, the circuit can be designed with the same methodology by simplifying the load to a pure resistor. The converter comprises three stages, viz., inverter stage, matching network stage, and rectifier stage. The inverter stage transfers the dc component into a high frequency ac component and the rectifier stage regulates the ac component into the dc output voltage. The matching network stage is adopted to adjust the equivalent impedance of the rectifier stage. Inductor $L_{\rm rec}$ represents the paralleled inductance of two inductors in matching network and rectifier stage, respectively.

The design starts from the rectifier stage. Once the rectifier stage is determined, it can be approximately represented by a certain impedance from a fundamental component perspective. Thereafter, the inverter stage and matching network stage can be designed based on a simpler equivalent model.

The diagram of the rectifier stage is shown in Fig. 2. To simplify the design procedure of the rectifier stage, the forward conduction voltage of the diode is ignored. The diode junction capacitance is absorbed by the resonant capacitor C_r. Input current of the rectifier stage can be approximately represented by a sinusoidal current source $i_S(t) = I_{\rm IN}\sin(\omega t + \varphi)$. For better accuracy, the Norton model will be adopted in the future work. The operating modes of the rectifier can be divided into two periods; during $0 < t < (1 - D)\,T$, the diode is OFF and during $(1 - D)\,T < t < T$, the diode is ON. Here, T is the operating period and D is the diode duty ratio (diode ON-time divided by period T).

When diode is OFF, based on Kirchhoff's voltage law, the voltage u_C across the diode can be represented by

$$\frac{d^2u_C\,(t)}{dt^2} + \frac{u_C\,(t)}{L_rC_r} = \frac{di_S\,(t)}{C_r dt} - \frac{V_{\rm LED} + I_O R_{\rm LED}}{L_rC_r} \tag{1}$$

where $V_{\rm LED}$ represents voltage drop and $R_{\rm LED}$ is the equivalent resistance. To reduce switching loss, the zero-current switching characteristics is expected, thus, the boundary conditions of (1) can be obtained

$$\begin{cases} u_C\,(t)\,|_{t=0} = u_C\,(t)\,\big|_{t=(1-D)T} = 0 \\ i_C\,(t)\,|_{t=0} = C_r \frac{du_C\,(t)}{dt}\Big|_{t=0} = 0 \end{cases}. \tag{2}$$

Substituting (2) into (1), u_C can be obtained as (3) shown when $0 \le t < (1 - D)T$. The voltage of diode is zero when diode is on during $(1 - D)T \le t \le T$

$$u_C\,(t) = \left(V_{\rm LED} + I_O R_{\rm LED} - \frac{I_{\rm IN}\omega L_r}{1 - \omega^2/{\omega_r}^2}\cos\varphi\right)\cos\left(\omega_r t\right) + \frac{I_{\rm IN}\omega L_r}{1 - \omega^2/{\omega_r}^2}\cos\left(\omega t + \varphi\right) - \left(V_{\rm LED} + I_O R_{\rm LED}\right) \tag{3}$$

where $\omega_r = 1/\sqrt{L_rC_r}$.

Furthermore, the following equations can be obtained:

$$\left(V_{\rm LED} + I_O R_{\rm LED}\right)\left[\cos\left(\omega_r\,(1 - D)\,T\right) - 1\right] + \frac{I_{\rm IN}\omega L_r}{1 - \omega^2/{\omega_r}^2} \times \cos\varphi\cos\left(\omega DT\right) = \frac{I_{\rm IN}\omega L_r}{1 - \omega^2/{\omega_r}^2}\cos\varphi \times \cos\left(\omega_r\,(1 - D)\,T\right) \tag{4}$$

$$\sin\varphi = 0. \tag{5}$$

Then, during the diode turn-OFF and turn-ON procedures, the current of inductor can be represented by the following

equations:

$$i_{L,\text{off}}(t) = I_{\text{IN}}\sin(\omega t+\varphi) + \frac{I_{\text{IN}}\omega L_r}{1-\omega^2/{\omega_r}^2}C_r\omega\sin(\omega t+\varphi) + \left(V_{\text{LED}} + I_O R_{\text{LED}} - \frac{I_{\text{IN}}\omega L_r}{1-\omega^2/{\omega_r}^2}\cos\varphi\right) \times C_r\omega_r\sin(\omega_r t) \quad (6)$$

$$i_{L,\text{on}}(t) = i_{L,\text{off}}(t)\big|_{t=(1-D)T} + \frac{V_{\text{LED}} + I_O R_{\text{LED}}}{L_r} \times [t-(1-D)T]. \quad (7)$$

During one period, according to the voltage seconds balance rule of inductor and the current seconds balance rule of capacitor, the following equations can be obtained:

$$\left(V_{\text{LED}} + I_O R_{\text{LED}} - \frac{I_{IN}\omega L_r}{1-\omega^2/{\omega_r}^2}\cos\varphi\right)\frac{1}{\omega_r} \times \sin(\omega_r(1-D)T) + (V_{\text{LED}} + I_O R_{\text{LED}})DT - \frac{I_{\text{IN}}L_r}{1-\omega^2/{\omega_r}^2} \times \sin(\omega DT)\cos\varphi = 0 \quad (8)$$

$$\frac{I_{\text{IN}}}{\omega}\cos\varphi[1-\cos(\omega DT)] - \frac{(V_{\text{LED}} + I_O R_{\text{LED}})D^2T^2}{2L_r} + I_O T = 0. \quad (9)$$

From the above analysis, it can be seen that there are nine parameters among (4), (5), (8), and (9), namely I_O, V_{LED}, R_{LED}, I_{IN}, ω, L_r, C_r, and D, φ. Once the load parameters, operating frequency and diode duty cycle are determined, the other four parameters can be calculated. The expressions of L_r and I_{IN} are shown as follows:

$$L_r = \frac{\left[K\left(1-\omega^2/{\omega_r}^2\right)(1-\cos(2\pi D))+2\pi^2D^2\right](V_{\text{LED}}+I_O R_{\text{LED}})}{2\pi\omega I_O} \quad (10)$$

$$I_{\text{IN}} = \frac{2\pi K\left(1-\omega^2/{\omega_r}^2\right)I_O}{\left[K\left(1-\omega^2/{\omega_r}^2\right)(1-\cos(2\pi D))+2\pi^2D^2\right]\cos\varphi}. \quad (11)$$

According to (4), (5), (8), and (12), K is defined as (12) shown, which is related with diode duty cycle D

$$K = \frac{\sin\left(2\pi\frac{\omega_r}{\omega}(1-D)\right)+2\pi D\frac{\omega_r}{\omega}}{\sin\left(2\pi\frac{\omega_r}{\omega}(1-D)\right)+\frac{\omega_r}{\omega}\sin(2\pi D)}. \quad (12)$$

B. Design of System Parameters

Based on above equations, a prototype with 12 V input voltage and 0.33 A constant output current is taken as an example to analyze the proposed topology. The operating frequency is set to be 20 MHz. Under above system specifications, the resonant inductor and capacitor value can be calculated as illustrated in Figs. 3 and 4, respectively. From Fig. 3, it can be seen that

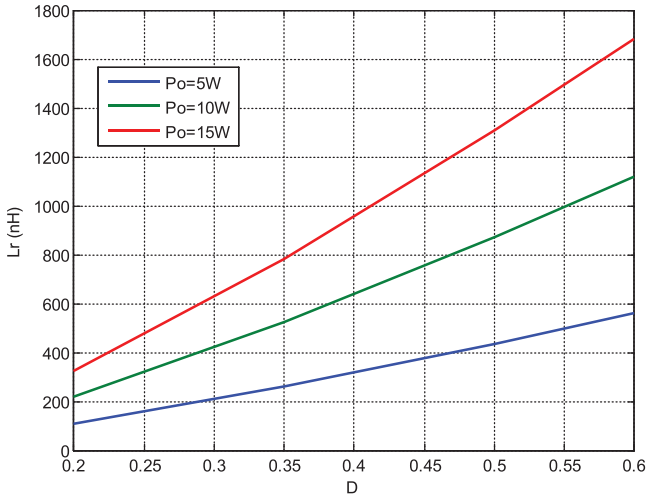


Fig. 3. Curve of resonant inductor in different load and duty cycle conditions. (Constant parameters: $f = 20$ MHz, $I_O = 0.33$ A).

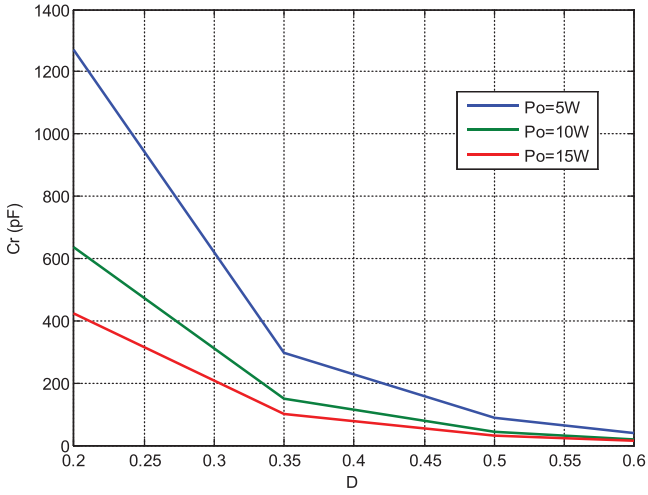


Fig. 4. Curve of resonant capacitor in different load and duty cycle conditions.(Constant parameters: $f = 20$ MHz, $I_O = 0.33$ A).

for a certain output power, the inductance forms a proportional relationship with the duty cycle. On the other hand, with the same duty cycle, the inductance increases in larger output power condition. For capacitance, the curves in Fig. 4 show an opposite conclusion as the inductance. It can be concluded from these two figures that a smaller duty cycle is expected in the system, because large duty cycle needs large inductance, which increases the volume and loss. Meanwhile, small capacitance puts a strict requirement for the parasitic capacitance of diode.

Fig. 5 shows the curves depicting inductance L_r in various output current and power conditions. The operating frequency and duty cycle keep in a constant value. It can be observed that the inductance decreases with the increment in output current I_O. It means that in the same output power condition, large output current is conducive to reduce the value of L_r, but larger current leads to more conduction loss. Furthermore, the inductance increases with the increment in output power in a constant I_O condition. Fig. 6 shows the curves of inductor L_r in various

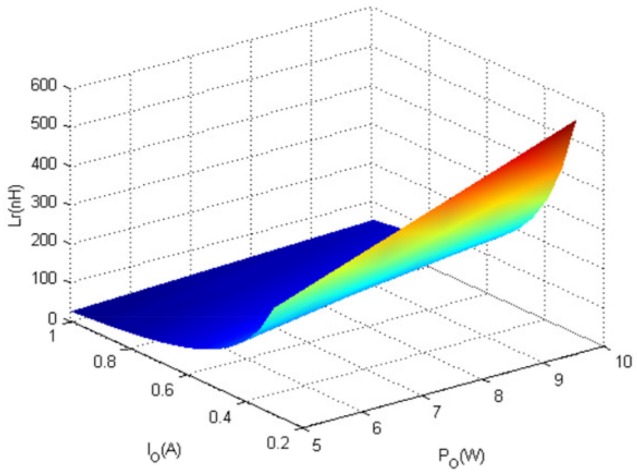


Fig. 5. Curves of inductor L_r in various output current and power conditions.(Constant parameters: $f = 20$ MHz, $D = 0.3$).

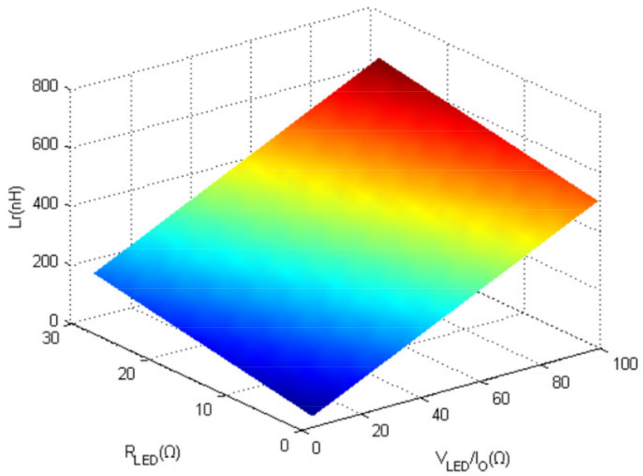


Fig. 6. Curves of inductor L_r in different R_{LED} and V_{LED}/I_o conditions. (Constant parameters: $f = 20$ MHz, $D = 0.3$).

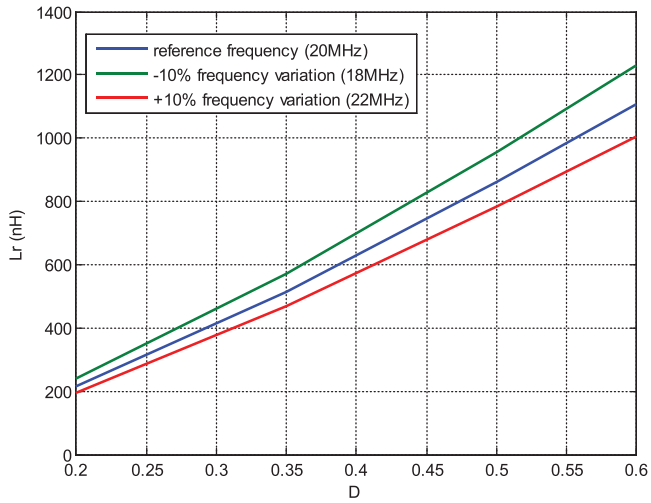


Fig. 7. Inductance curves under frequency variation conditions. (Constant parameters: $P_O = 9$ W, $I_O = 0.33$ A).

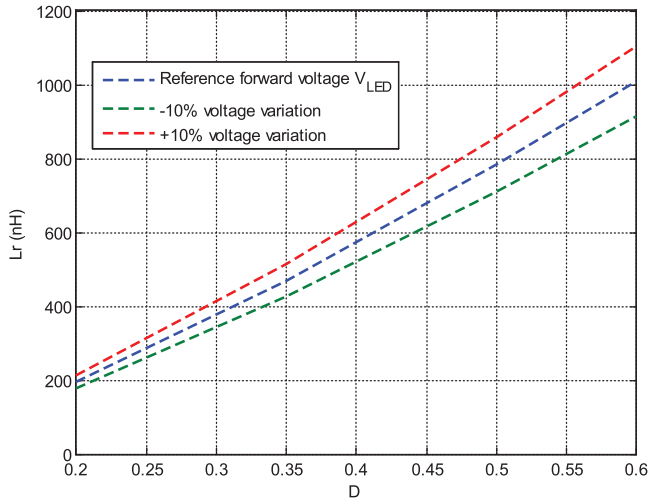


Fig. 8. Inductance curves under voltage V_{LED} variation conditions.(Constant parameters: $f = 20$ MHz, $R_{\mathrm{LED}} = 0.5\ \Omega$, $I_O = 0.33$ A).

load conditions. It can be seen that the value of inductor L_r forms a proportional relationship with the equivalent resistance R_{LED}. Furthermore, the value of L_r forms a proportional relationship with the ratio between the forward conduction voltage V_{LED} and current I_o.

Meanwhile, the effects of parameter variations should be taken into consideration. As shown in Fig. 7, a frequency variation of –10% leads to approximately 11% larger resonant inductors. On the other hand, a frequency variation of +10% leads to approximately 9% inductance discernment. The capacitance under frequency variations shows the same result as that of the inductance.

Fig. 8 shows the inductance curves under V_{LED} variation conditions, where the reference forward voltage is around 2.8 V. With a voltage variation of –10%, inductance reduced by 9%. On the other hand, an increment of +10% to the voltage also results in approximately 9% increase in inductance above the original value. Because of the unchanged operating frequency, the capacitance performs an opposite trend as that of inductance. The variation of resistance R_{LED} has the same effect as that of voltage V_{LED}.

Another very important property of the rectifier stage is the diode voltage stress. According to (3), the diode normalized voltage stress can be represented by the following equation:

$$U_{C,n} = U_{C-\max}/V_O = \max\left(\left|(1-K)\cos\left(\omega_r t\right)\right.\right. \\ \left.\left. + K\cos\left(\omega t\right) - 1\right|\right). \tag{13}$$

Fig. 9 shows the curves of the normalized diode voltage stress in various duty cycle conditions. It can be seen that small duty cycle helps to reduce the diode voltage stress. With a certain duty cycle, the inductance and capacitance can be calculated in a certain load condition. Then, the equivalent impedance of the rectifier stage can be approximately calculated based on the ratio between the fundamental voltage and the fundamental current.

Fig. 10 shows the topology equivalent circuit of the inverter and matching network stages. The equivalent resistance of the rectifier stage is represented by Z_R. The matching network is

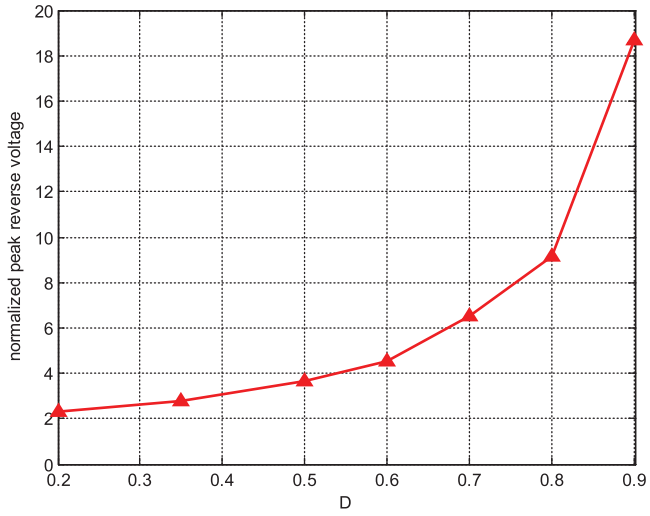


Fig. 9. Curve of normalized diode voltage stress in different *D* conditions.

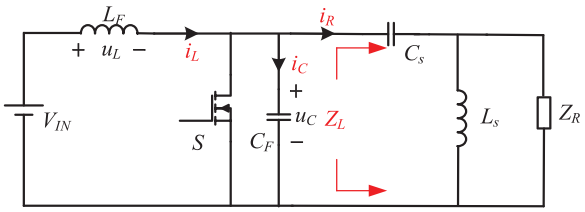


Fig. 10. Topology equivalent circuit including inverter and matching network.

composed of C_S and L_S. With the help of the matching network, the rectifier impedance Z_R can be adjusted to Z_L with two components' values shown in (14), to meet the output power requirement. Here, Z_L can be estimated by $Z_L = V_{DS}^2/P_o$

$$\begin{cases} L_s = \frac{Z_R}{\omega}\sqrt{\frac{Z_L}{Z_R - Z_L}} \\ C_s = \frac{1}{\omega\sqrt{Z_L(Z_R - Z_L)}} \end{cases}. \tag{14}$$

For the inverter stage, the current and voltage waveforms are shown in Fig. 11. The switch duty cycle is defined to be D_s. The operating mode of the inverter stage can be generally divided into two parts: when the switch turns-OFF at $t = 0$, the inductor and capacitor begin to resonate and voltage across the switch is larger than zero. At $t = (1 - D_s)T$ the switch voltage resonates back to zero, and this mode ends; then the switch turns-ON at $t = (1 - D_s)T$ with ZVS soft-switching characteristics. This mode ends at time $t = T$ and repeats again. When $0 < t < (1 - D_s)T$, the switch is OFF. The voltage across the switch can be represented by the following equation:

$$\frac{d^2u_C}{dt^2} + \frac{1}{Z_L C_F}\frac{du_C}{dt} + \frac{1}{L_F C_F}u_C = \frac{V_{\mathrm{IN}}}{L_F C_F}. \tag{15}$$

The switch is expected to operate in ZVS when the switch turns-ON. Thus, the initial condition can be represented by the

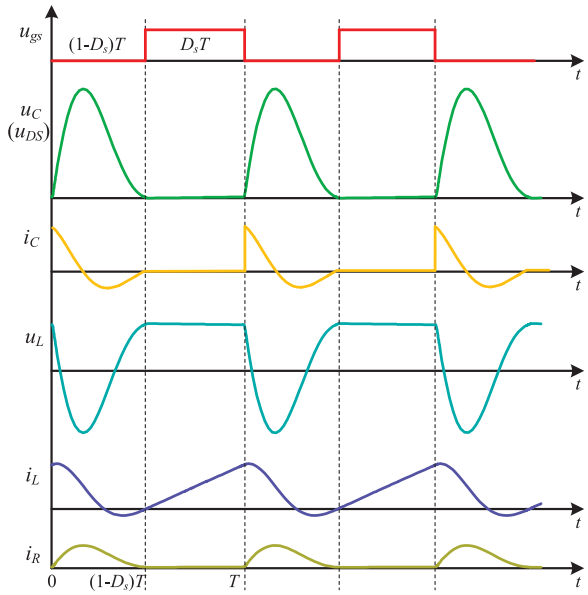


Fig. 11. Main current and voltage waveforms of the inverter stage.

following equation:

$$\begin{cases} u_C(0) = 0 \\ u_C\left((1 - D_s)T\right) = 0 \end{cases}. \tag{16}$$

Furthermore, one extra formula can be obtained by inductor volt-second balance principle. With a certain operating frequency and switch duty cycle, substituting these boundary conditions into (15), the relationship between the resonant frequency and operating frequency can be calculated. Usually, when the duty cycle is around 0.3 to 0.6, the frequency ratio between the resonant frequency and operating frequency is approximately 1.4 to 2. In addition, the impedance is expected to be inductive and with a phase angle θ around 30° to 60°. The phase angle forms a relationship with impedance parameters as shown in the following equation:

$$\tan(\theta) = \frac{Z_L}{\omega L_F} - C_F\omega Z_L. \tag{17}$$

Fig. 12 shows the impedance angle curves in various resonant inductor and capacitor conditions. It is evident that the impedance angle forms an almost proportional relationship with the value of C_F and an inversely proportional relationship with L_F. Based on the above calculation results, the final values can be obtained by slightly tuning parameters through simulation considering the effect of high-order harmonics.

III. Analysis and Design of Optimal Winding Structure

With small inductance in high frequency, the aircore inductors without magnetic core can be adopted. These inductors can be divided into several different categories, such as solenoid inductors and planar inductors. Commercial aircore inductors are usually in solenoid form that takes some vertical space of the system. For planar inductors, the copper tracks on PCB

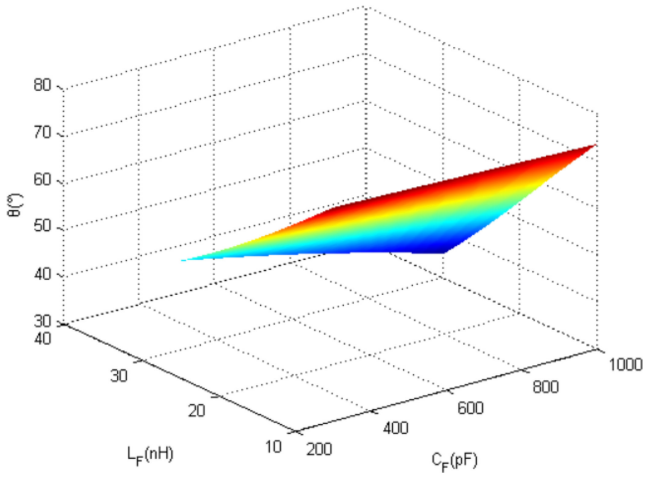


Fig. 12. Impedance angle curves with different inductor L_F and capacitor C_F.

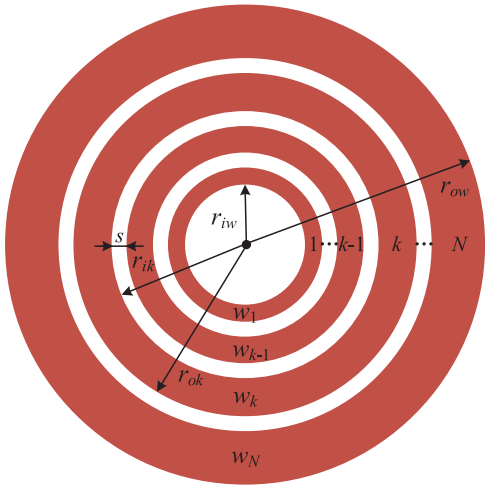


Fig. 13. Diagram of the variable width winding structure.

can be used as the windings. As a result, the aircore planar inductors do not take extra vertical space. In this paper, aircore planar inductors are chosen to reduce the system profile. There are many different winding shapes of planar inductors, such as square, hexagonal, and circular [29]. Among the several winding shapes, circular winding is the most widely used one. In high-frequency conditions, the winding resistance greatly increases. The variable width winding structure with wider tracks in the outer side shows smaller resistance characteristics compared with the constant width structure [33]. Based on this structure, an optimal structure of single-layer circular winding is designed to further reduce winding resistance and achieve a higher quality factor.

A. Analysis of the Winding Inductance

Fig. 13 shows the simplified diagram of the planar circular winding with various track widths. In this diagram, the inner radius, outer radius, and width of the kth turn are denoted as r_{ik}, r_{ok}, and w_k, respectively. The labels N, r_{iw}, r_{ow}, and s represent

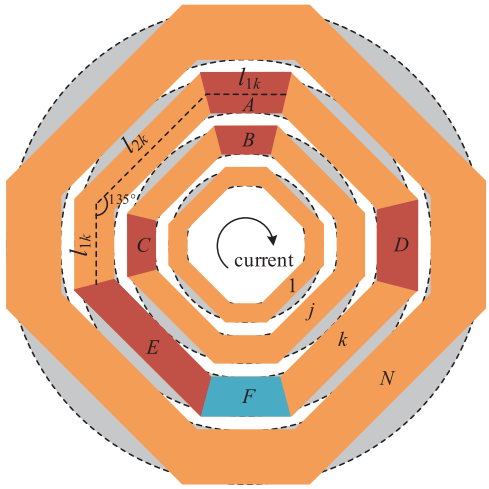


Fig. 14. Polygonal structure diagram of the winding.

the turn number of the winding, inner radius of the structure, outer radius of the structure, and the space between the turns, respectively.

In the beginning, the relationship between the inductance and structural parameters should be analyzed. To simplify the analysis, an approximate polygonal structure is adopted as shown in Fig. 14. It comprises a series of concentric quasi-regular octagons, and each quasi-regular octagon belongs to the kth turn with two edges l_{1k} and l_{2k}, which arrange alternately and intersect at an angle of 135°. To make the inductance of the equivalent model as close as possible to that of the original structure, perimeter of the octagon in the kth turn should be equal to that of the circle. Thus, l_{1k} and l_{2k} are obtained by (18), where radius ratio a is defined as $r_{\mathrm{ok}}/r_{\mathrm{ik}}$

$$\begin{cases} l_{1k} = 0.5346\left[r_{\mathrm{iw}} + (k-1.5)\,s + a^{k-1}\cdot\frac{(a-1)(r_{\mathrm{ow}}-r_{\mathrm{iw}}+s)}{2(a^N-1)}\right. \\ \qquad \left. + \sum_{i=1}^{k-1} a^{k-1}\cdot\frac{(a-1)(r_{\mathrm{ow}}-r_{\mathrm{iw}}+s)}{a^N-1} - s\right] \\ l_{2k} = 1.0362\left[r_{\mathrm{iw}} + (k-1.5)\,s + a^{k-1}\cdot\frac{(a-1)(r_{\mathrm{ow}}-r_{\mathrm{iw}}+s)}{2(a^N-1)}\right. \\ \qquad \left. + \sum_{i=1}^{k-1} a^{k-1}\cdot\frac{(a-1)(r_{\mathrm{ow}}-r_{\mathrm{iw}}+s)}{a^N-1} - s\right] \end{cases}. \tag{18}$$

The total inductance of a winding is the sum of the self-inductance of all the conductors and their mutual inductances. The self-inductance can be calculated by the following equation [30], [31]:

$$L_s = 0.8\sum_{k=1}^{N}\left\{\begin{array}{l} l_{1k}\left[\ln\left(\frac{l_{1k}}{a^{k-1}\cdot\frac{(a-1)(r_{\mathrm{ow}}-r_{\mathrm{iw}}+s)}{a^N-1}-s+t}\right)\right. \\ \qquad \left. + \frac{a^{k-1}\cdot\frac{(a-1)(r_{\mathrm{ow}}-r_{\mathrm{iw}}+s)}{a^N-1}-s+t}{3l_{1k}} + 0.94315\right] \\ +l_{2k}\left[\ln\left(\frac{l_{2k}}{a^{k-1}\cdot\frac{(a-1)(r_{\mathrm{ow}}-r_{\mathrm{iw}}+s)}{a^N-1}-s+t}\right)\right. \\ \qquad \left. + \frac{a^{k-1}\cdot\frac{(a-1)(r_{\mathrm{ow}}-r_{\mathrm{iw}}+s)}{a^N-1}-s+t}{3l_{2k}} + 0.94315\right] \end{array}\right\}. \tag{19}$$

As shown in Fig. 14, two major types of mutual inductance are considered. One of them is the mutual inductance between parallel conductors, such as conductors A and B or C and D, which can be calculated using the following equation [30], [31]:

$$\begin{aligned} M_{\text{para}} = 8 &\sum_{i=1}^{2}\sum_{j=1}^{N-1}\sum_{k=j+1}^{N} \\ &\times \left[M_p\left(\frac{l_{\text{ik}}+l_{\text{ij}}}{2}, r_k - r_j\right) - M_p\left(\frac{l_{\text{ik}}-l_{\text{ij}}}{2}, r_k - r_j\right)\right] \\ &- 4\sum_{i=1}^{2}\sum_{j=1}^{N}\sum_{k=1}^{N} \\ &\times \left[M_p\left(\frac{l_{\text{ik}}+l_{\text{ij}}}{2}, r_k + r_j\right) - M_p\left(\frac{l_{\text{ik}}-l_{\text{ij}}}{2}, r_k + r_j\right)\right] \end{aligned} \tag{20}$$

where the equation M_p satisfies (21) and M_p is in nanohenries, l and geometric mean distance (GMD) are in millimeters

$$M_p(l, \text{GMD}) = 0.2l\left[\ln\left(\frac{l}{\text{GMD}} + \sqrt{1+\left(\frac{l}{\text{GMD}}\right)^2}\right) - \sqrt{1+\left(\frac{\text{GMD}}{l}\right)^2} + \frac{\text{GMD}}{l}\right]. \tag{21}$$

The other is the mutual inductance between conductors connected at an angle of 135°, such as conductor E and F, which can be obtained according to the following equation:

$$\begin{aligned} M_\theta = 16 &\sum_{k=1}^{N} \frac{\sqrt{2}}{20}\left[(l_{1k}+l_{2k})\ln\right. \\ &\times \left(l_{1k}+l_{2k}+\sqrt{l_{1k}^2+l_{2k}^2-\sqrt{2}l_{1k}l_{2k}}\right) \\ &- l_{1k}\ln\left(l_{1k}-l_{2k}+\sqrt{l_{1k}^2+l_{2k}^2-\sqrt{2}l_{1k}l_{2k}}\right) \\ &\left.-l_{2k}\ln\left(l_{2k}-l_{1k}+\sqrt{l_{1k}^2+l_{2k}^2-\sqrt{2}l_{1k}l_{2k}}\right)\right]. \end{aligned} \tag{22}$$

Based on aforementioned analysis, inductance of the windings with different structure parameters can be calculated with the help of MATLAB. As shown in Fig. 15, the calculation results match well with the simulation results of FEA tools. Inductances form a proportional relationship with the inner radius, outer radius, and turns space. By changing these parameters, the expected inductor value can be achieved.

B. Optimal Design of the Winding Resistance

The winding resistance is also related with several parameters. One important parameter is how the radius ratio a is decided. Based on an intuitive hypothesis, the radius ratios $r_{\text{ok}}/r_{\text{ik}}$ in a certain winding should maintain a constant value, which may help to achieve the minimum resistance. Here, two simple structures with two and three turns are tested. For the two-turns

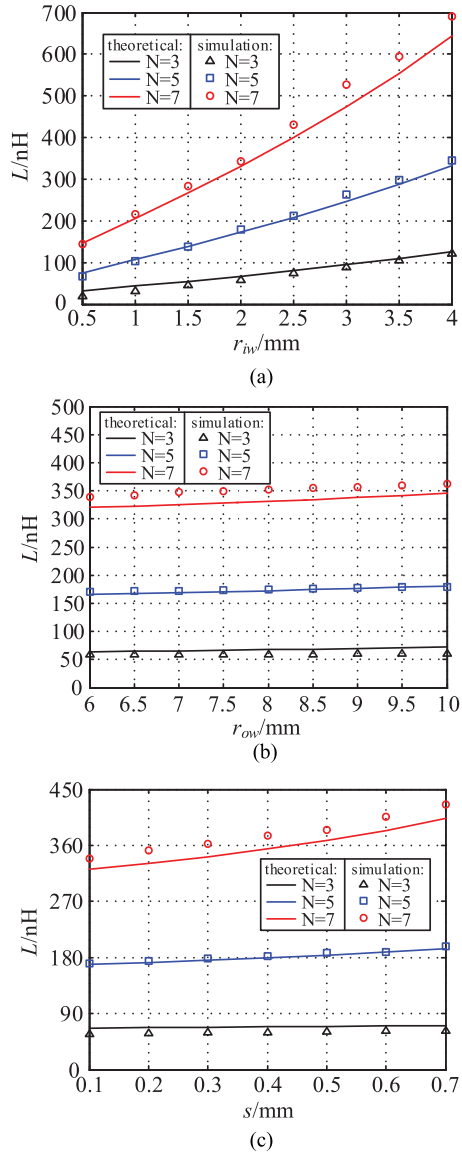


Fig. 15. Inductance in different structure parameter conditions. (a) Constant parameters: $r_{\text{ow}} = 8$ mm, $s = 0.2$ mm, $t = 0.072$ mm. (b) Constant parameters: $r_{\text{iw}} = 2$ mm, $s = 0.2$ mm, $t = 0.072$ mm. (c) Constant parameters: $r_{\text{iw}} = 2$ mm, $r_{\text{ow}} = 8$ mm, $t = 0.072$ mm.

condition, the radius ratio of first track is assumed to be a. Therefore, the inner radius of the second track can be calculated to be $ar_{\text{iw}} + s$ and the system resistance can be calculated as follows:

$$R_{2\text{turn}} = \frac{2\pi\rho}{t}\left(\frac{1}{\ln a} + \frac{1}{\ln\left(r_{\text{ow}}/(ar_{\text{iw}}+s)\right)}\right). \tag{23}$$

According to (23), the resistance is calculated as shown in Fig. 16. Here, r_{iw} is chosen to be 2 mm and r_{ow} is chosen to be 8 mm. The figure indicates that the resistance reaches its minimum value when the value of a is approximately 2. Furthermore, it can be calculated that the radius ratio of the second track is also 2, same as that of first track.

For the three-turns condition, the radius ratio of the first track is assumed to be a_1 and the radius ratio of the second track is assumed to be a_2. Thus, the inner radius of the third track can

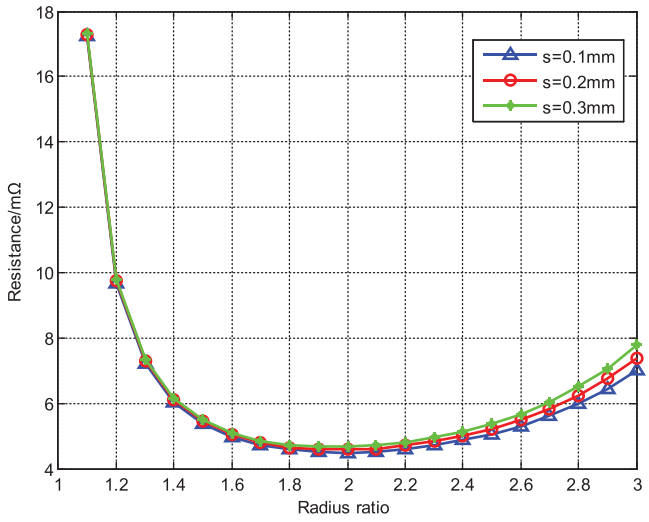


Fig. 16. Resistance under various radius ratio conditions (two-turns).

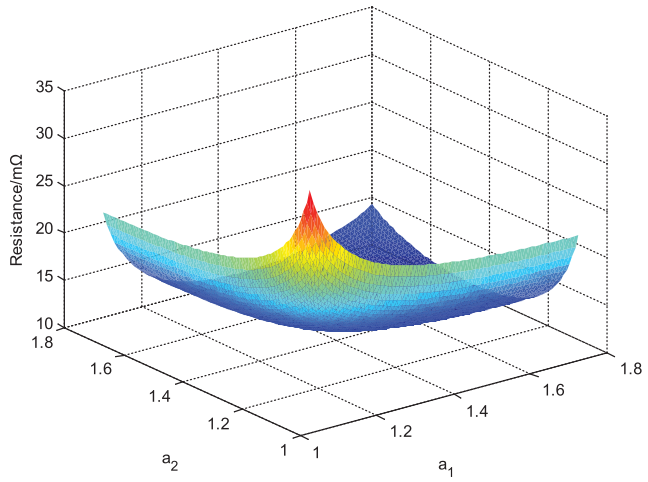


Fig. 17. Resistance under various radius ratio conditions (three-turns).

be calculated to be $a_1 a_2 r_{\rm iw} + a_2 s + s$ and the system resistance can be calculated as follows:

$$R_{3\rm turn} = \frac{2\pi\rho}{t} \times \left(\frac{1}{\ln a_1} + \frac{1}{\ln a_2} + \frac{1}{\ln\left(r_{\rm ow}/(a_2 a_1 r_{\rm iw} + a_2 s + s)\right)}\right). \quad (24)$$

According to (24), resistance of three turns is calculated as shown in Fig. 17. Here, $r_{\rm iw}$ is chosen to be 2 mm and $r_{\rm ow}$ is chosen to be 8 mm. It is identified that when a_1 is 1.57 and a_2 is 1.56, the resistance reaches its minimum value. In this condition, the radius ratio of the third track is calculated to be 1.56. It shows that a constant radius ratio can help to achieve the smallest winding resistance, which complies with the previous assumption.

Based on the above analysis, the radius ratio in different tracks is selected as the same value. In N turns situation, the optimal radius ratio can be calculated by the following equation:

$$a^N + a^{N-1}\frac{s}{r_{\rm iw}} + \cdots\cdots + a^2\frac{s}{r_{\rm iw}} + a\frac{s}{r_{\rm iw}} - \frac{r_{\rm ow}}{r_{\rm iw}} = 0. \quad (25)$$

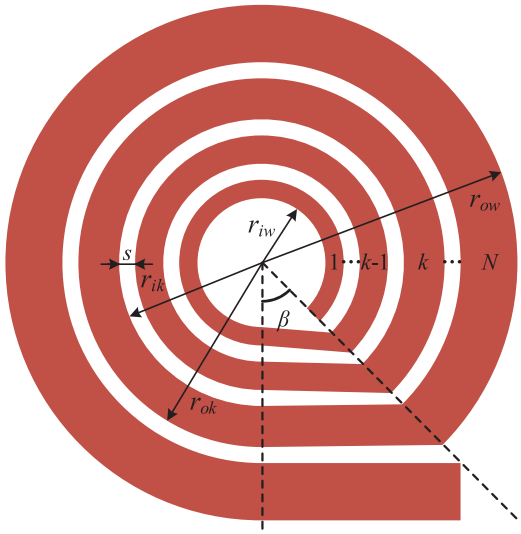


Fig. 18. Winding structure with transition straight conductor.

The above analysis is based on the usage of a simplified structure in an ideal condition. In actual situations, a transition straight conductor is needed to connect the adjacent turns. As shown in Fig. 18, the corresponding angle of the straight conductor is set to be a constant value β ($0 < \beta < \pi$). Here, an optimal value β should be calculated to achieve the minimum winding resistance.

Through integral calculation, it can be derived that the dc resistance of the arc in the kth turn is

$$R_{k\_(2\pi-\beta)} = \frac{(2\pi - \beta)\,\rho}{t \ln a} \quad (26)$$

where ρ is the resistivity of the conductor, and t is thickness of the winding. The dc resistance of the straight conductor in the kth turn can be calculated by the following equation:

$$R_{k\_\beta} = \frac{\rho\sqrt{1 + (a + a_s)^2 - 2\,(a + a_s)\cos\beta}}{t \ln\left(\frac{a+1}{2}\right)} \quad (27)$$

where $a_s = s/r_{\rm iw}$. Based on (26) and (27), the dc resistance of the whole winding can be calculated.

In high-frequency ac conditions, influenced by the skin effect, current is mainly distributed in the conductor surface reducing the effective cross-sectional area of the conductor, significantly increasing the winding resistance. The work in [32] gives an empirical formula for calculating high-frequency resistance of the windings caused by the skin effect, the ac resistance is derived as follows:

$$R_{\rm ac} = \frac{\xi}{2}\cdot\frac{\sinh\xi + \sin\xi}{\cosh\xi - \cos\xi}\cdot\frac{N\rho}{t} \cdot \left(\frac{2\pi - \beta}{\ln a} + \frac{\sqrt{1 + (a + a_s)^2 - 2\,(a + a_s)\cos\beta}}{\ln\left(\frac{a+1}{2}\right)}\right) \quad (28)$$

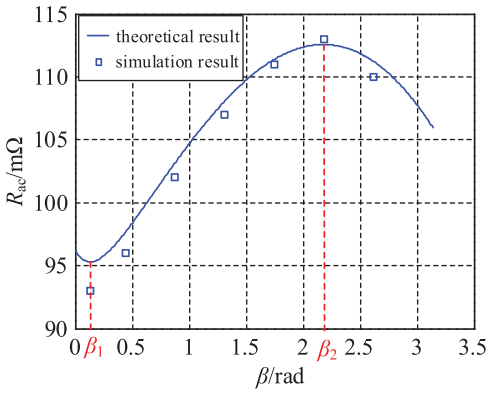


Fig. 19. Curve of winding ac resistance in different β conditions.

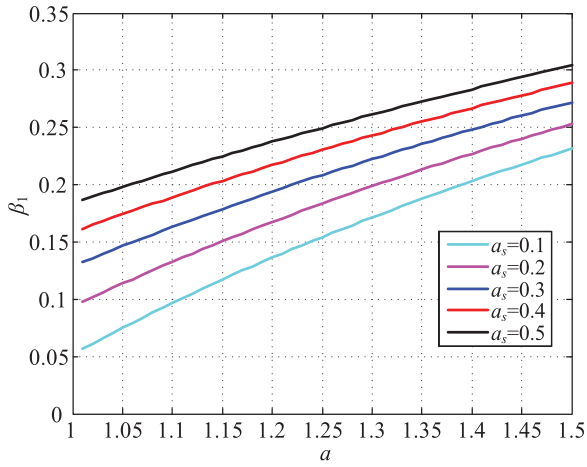


Fig. 20. Curves of β_1 related with a and a_s.

where $\xi = t\sqrt{\pi f \mu \sigma}$, f is the frequency of the ac current, μ and σ are the permeability and the conductivity of the conductor, respectively.

To optimize the design of β and minimize the winding resistance, the derivative of (28) is calculated.

Setting the derivative value be zero, the extreme points are obtained as follows:

$$\begin{cases} \beta_1 = \arccos \dfrac{\ln^2\left(\frac{a+1}{2}\right)+\sqrt{\ln^4\left(\frac{a+1}{2}\right)-\ln^2 a\left[\left(\ln^2\left(\frac{a+1}{2}\right)-\ln^2 a\right)(a+a_s)^2+\ln^2\left(\frac{a+1}{2}\right)\right]}}{(a+a_s)\ln^2 a} \\ \beta_2 = \arccos \dfrac{\ln^2\left(\frac{a+1}{2}\right)-\sqrt{\ln^4\left(\frac{a+1}{2}\right)-\ln^2 a\left[\left(\ln^2\left(\frac{a+1}{2}\right)-\ln^2 a\right)(a+a_s)^2+\ln^2\left(\frac{a+1}{2}\right)\right]}}{(a+a_s)\ln^2 a} \end{cases} . \tag{29}$$

It can be proved from further mathematical analysis that R_{ac} reaches its minimum in β_1 and maximum in β_2. It implies that β_1 is the best design choice. Fig. 19 also shows the value of the resistance with various values of β when $r_{iw} = 2$ mm, $r_{ow} = 6$ mm, $N = 5$, and $s = 0.2$ mm ($a = 1.1886$, $a_s = 0.1$) to verify the correctness of the above analysis.

From Fig. 19, it is evident that the winding resistance increases with the increment of angle when it is between β_1 and β_2. The resistance achieves the minimum value at β_1 which is consistent with the above analysis, which agrees with simulation results. Fig. 20 shows the curves of β_1 with different a and a_s. It can be seen that β_1 forms an approximately proportional relationship with a, and β_1 also increases with the increment of a_s. Based on the optimal a and β, the aircore inductor with the expected value and small ac resistance can be designed.

IV. Experimental Results

Based on the proposed topology and winding structure, a 9 W dc–dc converter for LED driving system is designed in this paper. The input voltage is 12 V and the output voltage is 27 V. The operating frequency is set to be 20 MHz. Based on the design method of the proposed converter, the system parameters can be calculated, as shown in Table I. In the prototype, the sum of the discrete paralleled capacitor and switch output parasitic capacitor is taken as the resonant capacitor. The parasitic capacitance varies when selecting different type switches and packages. Thus, to compensate parasitic capacitance variation, the paralleled discrete capacitor can be slightly tuned to modify the performance. For a certain inductance with expected size and quality factor, winding structure design starts from the inductance expressions of (18)–(22). The inductance curves indicate that winding turns number plays a dominant role of determining the inductance. Then, by adjusting the inner radius, outer radius, and space, the specific inductance can be achieved. Based on the certain inner/outer radius and space, the angle can be optimized by (29). In addition, another 12 V input, 5 V/10 W output dc–dc prototype for auxiliary power supply is also built.

TABLE I
Parameters of the Proposed Converter

Symbol	Description	Value/Type
C_F	Resonant capacitor	390 pF
L_F	Resonant inductor	56 nH (s=0.2 mm, t=0.072 mm, a=1.26, β=11°, n=3, r_{iw}=1.7 mm, r_{ow}=4 mm)
C_s	Resonant capacitor	330 pF
C_o	Output capacitor	4.7 uF*6
S	Switch	SI7454
D	Diode	STPS2H100A
C_r	Resonant capacitor	150 pF
L_{rec}	Parallel of L_r and L_s	110 nH (s=0.2 mm, t=0.072 mm, a=1.2, β=10°, n=5, r_{iw}=1.3 mm, r_{ow}=4.5 mm)

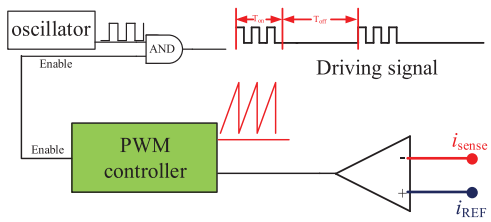


Fig. 21. Diagram of the PWM type ON/OFF control method.

Fig. 21 depicts the PWM type ON/OFF control method of the proposed converter. The 20 MHz high-frequency signal is

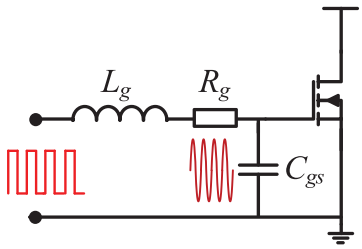


Fig. 22. Diagram of the resonant driving circuit.

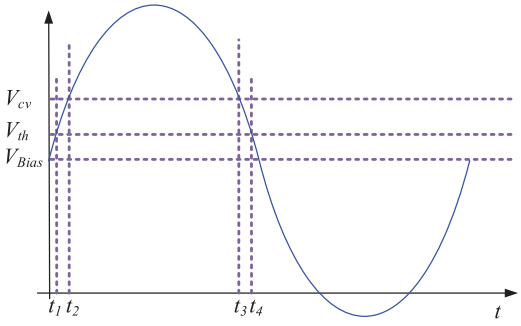


Fig. 23. Resonant driving voltage waveform.

modulated with the enable signal by an AND gate. When enable signal is high, the 20 MHz signal passes through the AND gate and the output capacitor is charged. When enable signal is low, the output of the AND gate keeps low and the output capacitor discharges to the load. Thus, the effective operating time of the system can be adjusted by changing the duty cycle of the enable signal. Furthermore, as shown in Fig. 22, in the driving circuit, a resonant inductor is added in series with the switch gate, which can resonate with the switch input capacitance to make use of the capacitor-stored energy. The resonant driving method can reduce the driving loss. However, it increases the switch conduction loss. Fig. 23 shows the resonant driving waveforms. At t_1, the driving voltage reaches the threshold voltage $v_{\rm th}$ and the switch turns-ON. At t_2, the driving voltage reaches the critical voltage $v_{\rm cv}$, then the switch is fully turned ON.

As shown in the switch datasheets, when the driving voltage is between the threshold voltage and critical voltage, the switch ON-resistance is in a high value condition. After the driving voltage is higher than the critical voltage, the switch ON-resistance significantly reduces and also remains constant. Compared with the square-wave driving method, the transition time between the threshold voltage and critical voltage is longer in the resonant driving method.

The driving loss of the square-wave driving method can be approximately calculated as follows:

$$P_{\rm square} = C_{gs} V_{gs}^2 f. \tag{30}$$

The driving loss of the resonant driving method can be approximately calculated as follows:

$$P_{\rm resonant} = 2\pi^2 f^2 V_{\rm gs}^2 C_{\rm gs}^2 R_g. \tag{31}$$

Here, the switch average current within time t_1 to t_4 is defined as $I_{\rm avg}$, ON-resistance between transition times t_1 to t_2 and t_3 to t_4 is defined as $R_{\rm tra}$, and ON-resistance between fully turned-ON time t_2 to t_3 is defined as $R_{\rm on}$. The period is represented by T. The switch conduction loss of the square-wave driving method can be approximately calculated as follows:

$$P_{\rm on\_square} = I_{\rm avg}^2 R_{\rm on} \frac{(t_4 - t_1)}{T}. \tag{32}$$

The switch conduction loss of the resonant driving method can be approximately calculated as follows:

$$P_{\rm on\_resonant} = I_{\rm avg}^2 R_{\rm tra} \frac{2\,(t_2 - t_1)}{T} + I_{\rm avg}^2 R_{\rm on} \frac{(t_3 - t_2)}{T}. \tag{33}$$

Under 20 MHz condition, the sum of the switch conduction loss and driving loss under different switch average current conditions is shown in Fig. 24. It can be seen that there is a cross point of these two loss curves. It can be concluded that when system switch current is small, the resonant driving method is conducive to improve the system efficiency. On the other hand, when system is in a high current condition, the square-wave driving method should be adopted.

Fig. 25 shows the diode voltage waveforms of the rectifier stage. The duty cycle of the diode is approximately 0.35 and the stress is approximately three times of the output voltage. Fig. 26 shows the switch drain-to-source voltage and the driving voltage. The switch can operate in the ZVS condition and the driving signal is in sinusiodal form with the resonant driving

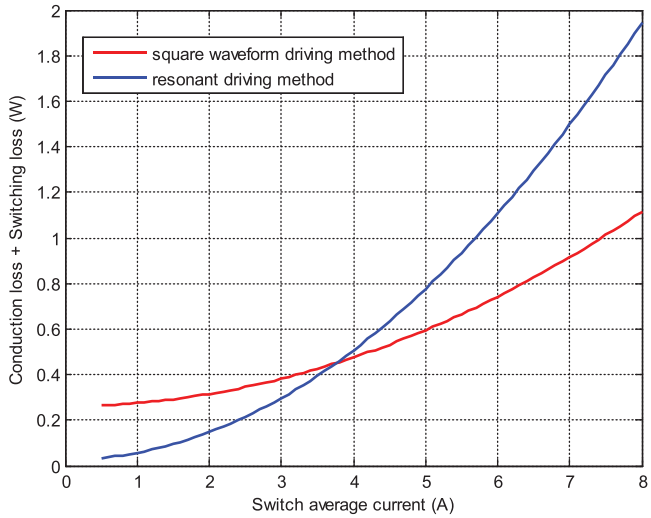


Fig. 24. Conduction and driving loss with two driving methods (20 MHz).

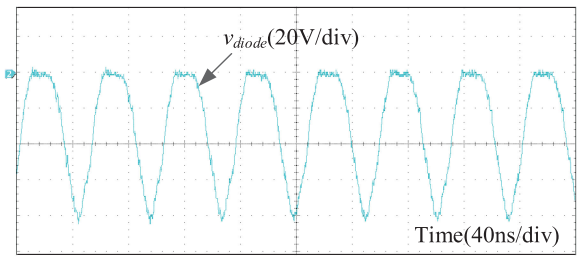


Fig. 25. Voltage waveform across the diode.

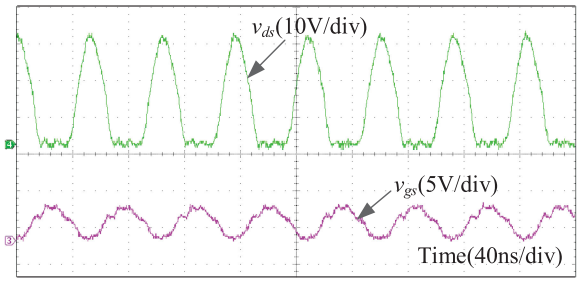


Fig. 26. Switch drain-to-source voltage and driving voltage.

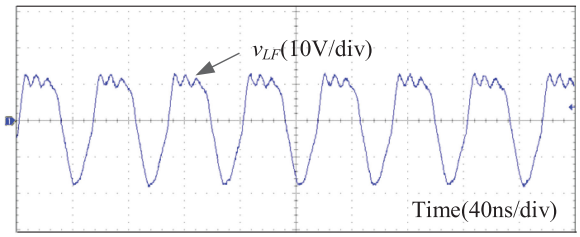


Fig. 27. Voltage of inductor L_F.

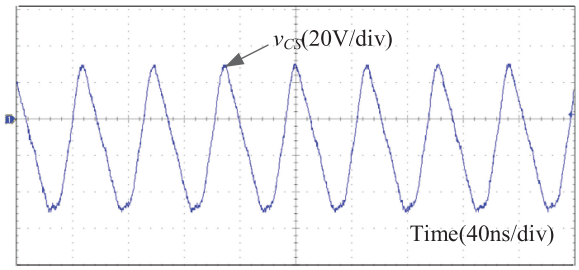


Fig. 28. Voltage of capacitor C_S.

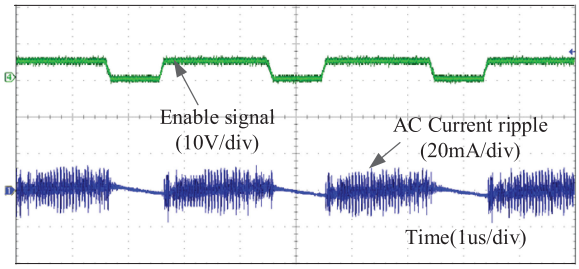
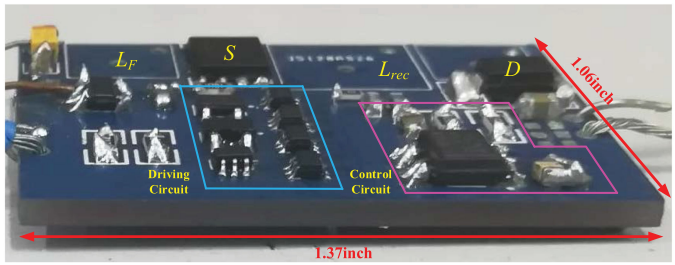


Fig. 29. Enable signal and ac ripple of output current.

method. The voltage waveforms of the inductor L_F and the capacitor C_S are depicted in Figs. 27 and 28, respectively. Fig. 29 shows the current ripple is approximately 20 mA, which is 5% of the output current. Smaller output ripple can be achieved by either improving the ON/OFF control frequency or increasing the output capacitance. Fig. 30 shows the top and side view of the prototype, the height of the system is 0.157 in, and the power density is as high as 39.13 W/in^3.

In a rated output condition, the efficiency is 90% and the loss breakdown is shown in Fig. 31. For 12–5 V application, the switch and diode waveforms are shown in Fig. 32. With the same design method, they can also achieve soft-switching



(a)

(b)

Fig. 30. Top and side photographs of the prototype. (a) Top view. (b) Side view.

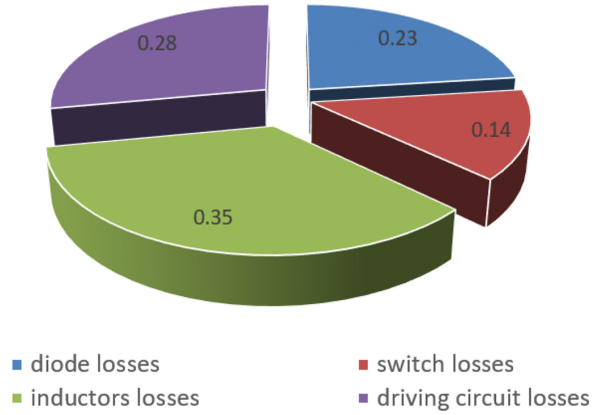
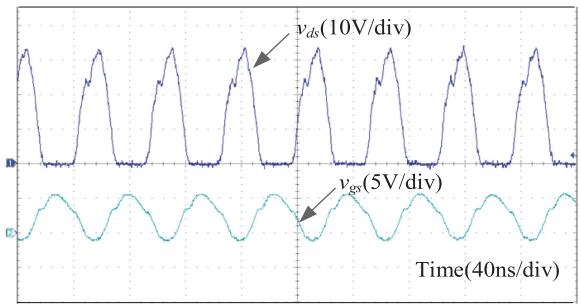
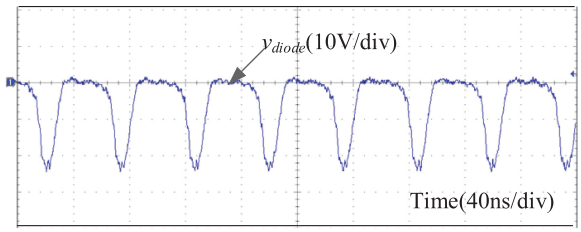


Fig. 31. Losses dissipation of the prototype.



(a)



(b)

Fig. 32. Waveforms of 12–5 V prototype. (a) Switch drain-to-source voltage and driving voltage. (b) Voltage across diode.

TABLE II
PROPERTIES COMPARISONS BETWEEN DIFFERENT TOPOLOGIES

Topology	f_s	Switch number	Diode number	Output power (W)	Efficiency	Height (in)	Power density (W/in^3)
Proposed	20 MHz	1	1	9	90%	0.157	39.13
ZVS Cuk [18]	2.4 MHz	2	0	30	92.9%	0.394	21.99
Boost	1 MHz	1	1	10	92%	0.63	10.83
Double LLC [19]	120 kHz	2	2	30	92%	0.787	10.4
Coupled Cuk [20]	500 kHz	1	1	40	89.7%	0.317	N.A.
LT3761 [21]	350 kHz	1	1	40	90%	0.295	N.A.
Integrated-magnetics Cuk [22]	1.8 MHz	2	0	30	85%	0.394	16.39

TABLE III
PARAMETERS OF THE PROPOSED CONVERTER (10 MHz)

Symbol	Value/Type	Package
C_F	1000 pF/50 V	0603 (1.60 mm x 0.80 mm)
L_F	110 nH	n=5, r_{iw}=1.2 mm, r_{ow}=5.5 mm
C_s	680 pF/50 V	0603 (1.60 mm x 0.80 mm)
C_r	390 pF/100 V	0805 (2.01 mm x 1.25 mm)
L_{rec}	210 nH	n=7, r_{iw}=0.9 mm, r_{ow}=10.8 mm

modes. Table II lists some high-frequency state-of-the-art dc–dc converters. High magnetic loss and negative effect of parasitic components are the bottlenecks of further improving their operating frequency to tens of Megahertz. It can be seen that with 20 MHz operating frequency and aircore inductor, the proposed converter has the lowest profile.

If the operating frequency reduces to 10 MHz, the capacitors C_F, C_S, and C_r will be 1000, 680, and 390 pF; the inductors L_F and $L_{\rm rec}$ will increase to 110 nF and 210 nH. As shown Table III, the capacitor size can be kept almost the same. To keep the same winding resistance, the aircore inductors are redesigned. Compared with the outer radius, the size of L_F increases about 1.9 times and the size of $L_{\rm rec}$ increases about 5.8 times, which greatly reduces the system power density. In further work, the proposed converter is going to be modified into an isolated one by inserting an air core transformer between the inverter and rectifier stage.

V. CONCLUSION

This paper proposed a low-profile high-frequency dc–dc converter. An optimal parameter design method was analyzed, which guaranteed the switch and diode operating in the soft-switching modes. Air core inductors with magnetic-free characteristics significantly reduced the need for system vertical space. The systematic design method of winding structure contributed to lower winding resistances. A 20 MHz prototype was built, which verified the feasibility of the proposed topology and design strategies. The power density could be as high as 39.13 W/in^3 and the efficiency was 90%.

REFERENCES

[1] M. Sharifzadeh, H. Vahedi, R. Portillo, L. Garcia Franquelo, and K. Al-Haddad, "Selective harmonic mitigation-based self-elimination of triplen harmonics for single-phase five-level inverters," *IEEE Trans. Power Electron.*, vol. 34, no. 1, pp. 86–96, Jan. 2019.
[2] J. Napoles *et al.*, "Selective harmonic mitigation technique for cascaded H-bridge converters with nonequal DC link voltages," *IEEE Trans. Ind. Electron.*, vol. 60, no. 5, pp. 1963–1971, May 2013.
[3] J. M. Alonso, M. S. Perdigão, M. A. Dalla Costa, G. Martínez, and R. Osorio, "Analysis and experiments on a single-inductor half-bridge LED driver with magnetic control," *IEEE Trans. Power Electron.*, vol. 32, no. 12, pp. 9179–9190, Dec. 2017.
[4] J. Liu, Y. Yin, W. Luo, S. Vazquez, L. G. Franquelo, and L. Wu, "Sliding mode control of a three-phase AC–DC voltage source converter under unknown load conditions: Industry applications," *IEEE Trans. Syst., Man, Cybern., Syst.*, vol. 48, no. 10, pp. 1771–1780, Oct. 2018.
[5] J. I. Leon, S. Vazquez, and L. G. Franquelo, "Multilevel converters: Control and modulation techniques for their operation and industrial applications," *Proc. IEEE*, vol. 105, no. 11, pp. 2066–2081, Nov. 2017.
[6] J. M. Alonso, M. S. Perdigão, G. Z. Abdelmessih, M. A. Dalla Costa, and Y. Wang, "SPICE modeling of variable inductors and its application to single inductor LED driver design," *IEEE Trans. Ind. Electron.*, vol. 64, no. 7, pp. 5894–5903, Jul. 2017.
[7] A. K. Yadav, M. Boby, S. K. Pramanick, K. Gopakumar, L. Umanand, and L. G. Franquelo, "Generation of high-resolution 12-sided voltage space vector structure using low-voltage stacked and cascaded basic inverter cells," *IEEE Trans. Power Electron.*, vol. 33, no. 9, pp. 7349–7358, Sep. 2018.
[8] S. Vazquez, A. Marquez, R. Aguilera, D. Quevedo, J. I. Leon, and L. G. Franquelo, "Predictive optimal switching sequence direct power control for grid-connected power converters," *IEEE Trans. Ind. Electron.*, vol. 62, no. 4, pp. 2010–2020, Apr. 2015.
[9] X. Xie, J. Wang, C. Zhao, Q. Lu, and S. Liu, "A novel output current estimation and regulation circuit for primary side controlled high power factor single-stage flyback LED driver," *IEEE Trans. Power Electron.*, vol. 27, no. 11, pp. 4602–4612, Nov. 2012.
[10] Y. C. Chuang, Y. L. Ke, H. S. Chuang, and C. C. Hu, "Single-stage power factor-correction circuit with flyback converter to drive LEDs for lighting applications," in *Proc. Rec. IEEE IAS Annu. Meeting*, 2010, pp. 1–9.
[11] S. Moon, G. B. Koo, and G. W. Moon, "A new control method of interleaved single-stage flyback ac–dc converter for outdoor LED lighting systems," *IEEE Trans. Power Electron.*, vol. 28, no. 8, pp. 4051–4062, Aug. 2013.

[12] J. Warren, K. Rosowski, and D. Perreault, "Transistor selection and design of a VHF DC-DC power converter," *IEEE Trans. Power Electron.*, vol. 23, no. 1, pp. 27–37, Jan. 2008.

[13] B. Lin, C. Huang, and H. Chiang, "Analysis of a soft switching PWM active clamp Cuk converter," in *Proc. 2nd IEEE Conf. Ind. Electron. Appl.*, Harbin, China, 2007, pp. 2311–2316.

[14] R. Gules, W. M. Santos, F. A. Reis, E. F. R. Romaneli, and A. A. Badin, "A modified SEPIC converter with high static gain for renewable applications," *IEEE Trans. Power Electron.*, vol. 29, no. 11, pp. 5860–5871, Nov. 2014.

[15] C. M. Lai and K. K. Shyu, "A single-stage ac–dc converter based on zero voltage switching LLC resonant topology," *IET Elect. Power Appl.*, vol. 152, no. 3, pp. 743–752, Sep. 2007.

[16] J. M. Burkhart, R. Korsunsky, and D. J. Perreault, "Design methodology for a very high frequency resonant boost converter," *IEEE Trans. Power Electron.*, vol. 28, no. 4, pp. 1929–1937, Apr. 2013.

[17] J. Hu, "Design of a low-voltage low-power dc–dc HF converter," *M.S. thesis*, Dept. Elect. Eng. Comput. Sci., Massachusetts Inst. Technol., Cambridge, MA, USA, 2008.

[18] A. Sepahvand, M. Doshi, V. Yousefzadeh, J. Patterson, K. K. Afridi, and D. Maksimović, "High-frequency ZVS Ćuk converter for automotive LED driver applications using planar integrated magnetics," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Tampa, FL, USA, 2017, pp. 2467–2474.

[19] Y. Wang, S. Gao, Y. Guan, J. Huang, D. G. Xu, and W. Wang, "A single-stage LED driver based on double LLC resonant tanks for automobile headlight with digital control," *IEEE Trans. Transp. Electrification*, vol. 2, no. 3, pp. 357–368, Sep. 2016.

[20] L. Corradini and G. Spiazzi, "A high-frequency digitally controlled LED driver for automotive applications with fast dimming capabilities," *IEEE Trans. Power Electron.*, vol. 29, no. 12, pp. 6648–6659, Dec. 2014.

[21] Linear Technologies, LT3761A Technical Datasheet, 2016. [Online]. Available: https://cds.linear.com/docs/en/datasheet/3761af.pdf

[22] A. Sepahvand, M. Doshi, V. Yousefzadeh, J. Patterson, K. Afridi, and D. Maksimovic, "Automotive LED driver based on high frequency zero voltage switching integrated magnetics Cuk converter," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2016, pp. 1–8.

[23] A. D. Sagneri, D. I. Anderson, and D. J. Perreault, "Optimization of integrated transistors for very high frequency DC–DC converters," *IEEE Trans. Power Electron.*, vol. 28, no. 7, pp. 3614–3626, Jul. 2013.

[24] J. Hu, A. D. Sagneri, J. M. Rivas, Y. Han, S. M. Davis, and D. J. Perreault, "High-frequency resonant SEPIC converter with wide input and output voltage ranges," *IEEE Trans. Power Electron.*, vol. 27, no. 1, pp. 189–200, Jan. 2012.

[25] D. Reusch and J. Strydom, "Evaluation of gallium nitride transistors in high frequency resonant and soft-switching DC–DC converters," *IEEE Trans. Power Electron.*, vol. 30, no. 9, pp. 5151–5158, Sep. 2015.

[26] D. Reusch and J. Glaser, *DC-DC Converter Handbook – A Supplement to GaN Transistors for Efficient Power Conversion*, 1st ed. El Segundo, CA, USA: Efficient Power Convers. Publications, 2015.

[27] J. Glaser, J. Strydom, and D. Reusch, "High power fully regulated eighth-brick DC-DC converter with GaN FETs," in *Proc. Int. Conf. Power Electron. Intell. Motion Renewable Energy Energy Manage.*, 2015, pp. 1–8.

[28] C. Quinn, K. Rinne, T. O'Donnell, M. Duffy, and C. O. Mathuna, "A review of planar magnetic techniques and technologies," in *Proc. 16th Annu. IEEE Appl. Power Electron. Conf. Expo.*, 2001, pp. 1175–1183.

[29] S. S. Mohan, M. del Mar Hershenson, S. P. Boyd, and T. H. Lee, "Simple accurate expressions for planar spiral inductances," *IEEE J. Solid-State Circuits*, vol. 34, no. 10, pp. 1419–1424, Oct. 1999.

[30] F. E. Terman, *Radio Engineer's Handbook*. New York, NY, USA: McGraw-Hill, 1943.

[31] H. Greenhouse, "Design of planar rectangular microelectronic inductors," *IEEE Trans. Parts, Hybrids, Packag.*, vol. 10, no. 2, pp. 101–109, Jun. 1974.

[32] Z. Ouyang and M. A. E. Andersen, "Overview of Planar Magnetic Technology—Fundamental Properties," *IEEE Trans. Power Electron.*, vol. 29, no. 9, pp. 4888–4900, Sep. 2014.

[33] X. Huang and K. D. T. Ngo, "Design technique for a spiral planar winding with geometric radii," *IEEE Trans. Aerosp. Electron. Syst.*, vol. 32, no. 2, pp. 825–830, Apr. 1996.

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